CLAIMS

What is claimed is:

1. A computer system that comprises:

an expansion bus that includes a plurality of expansion bus signals;

a bus bridge coupled to the expansion bus; and

a signal gate configurable to isolate the bus bridge from one of the expansion bus signals.

2. The computer system of claim 1, further comprising:

a controller configured to receive said one of the expansion bus signals and configured to determine whether said one of the expansion bus signals is driven in a non-standard manner, wherein the controller sets the signal gate to isolate the bus bridge from the expansion bus signal if the controller determines that the expansion bus signal is driven in a non-standard manner.

3. The computer system of claim 2, wherein said one of the expansion bus signals is a wake-up signal.

4. The computer system of claim 2, wherein said bus bridge is the south bridge.

5. The computer system of claim 2, wherein said one of the expansion bus signals is a power management event (PME#) signal, and wherein said controller determines that the PME# signal is driven in a non-standard manner if the PME# signal is determined to be low at a predetermined time delay after a Power Good signal goes low.

6. The computer system of claim 2, wherein the controller is a power management controller.

7. A computer system that comprises:

a user input device;

a computer chassis that contains at least:

a system memory configured to store an operating system;

a central processor coupled to the memory and configured to execute the operating system;

an expansion bus that couples the user input device to the central processor;

a bus bridge coupled to the expansion bus, wherein the bus bridge includes:

a power management controller coupled to the expansion bus and configured to receive a wake-up signal from a device resident on the expansion bus, wherein the power management controller isolates the wake-up signal from the bus bridge device if the device drives the wake-up signal in a non-compliant manner.

8. The computer system of claim 7, wherein the bus bridge is a south bridge.

9. The computer system of claim 7, wherein the wake-up signal is a power management event (PME#) signal, and wherein the controller isolates the PME# signal from the bus bridge if the PME# signal is low following a predetermined delay after a Power Good signal is de-asserted.

10. The computer system of claim 9, further comprising:

a signal gate that couples the wake-up signal to the bus bridge, wherein the signal gate is set to a "pass" state by the controller if the PME# signal is high following after a predetermined delay following the de-assertion of the Power Good signal, and wherein the signal gate is set by the controller to a "no-pass" state otherwise.

11. A method for handling non-compliant devices in a computer, wherein the method comprises:

detecting a transition of the computer to a reduced-power state;

pausing for a predetermined delay;

sampling one or more wake-up signals from one or more devices;

establishing a signal block against any asserted wake-up signals.

12. The method of claim 11, further comprising:

removing any signal blocks against sampled wake-up signals that are de-asserted.

13. The method of claim 11, wherein said detecting includes:

monitoring a Power Good signal; and

sensing a transition of the Power Good signal from an asserted state to a de-asserted state.

14. The method of claim 11, wherein the one or more wake-up signals are power management event (PME#) signals from devices resident on a peripheral component interconnect (PCI) bus.

15. The method of claim 11, wherein the establishing includes:

setting a signal gate to isolate the asserted wake-up signals from a bus bridge.

16. A computer system that comprises:

an expansion bus that includes a plurality of expansion bus signals;

a bus bridge coupled to the expansion bus; and

a controller coupled to receive at least one of the expansion bus signals and configured to provide a gated signal to the bus bridge, wherein the gate signal is asserted only if an received expansion bus signal is asserted and not blocked.

17. The computer system of claim 16, wherein the controller determines whether the received signals are driven in a non-standard manner, and wherein the controller blocks any received expansion bus signals that the controller determines are driven in a non-standard manner.

18. The computer system of claim 16, wherein the received expansion bus signals are wake-up signals.

19. The computer system of claim 16, wherein the receive expansion bus signals are power management event (PME#) signals, and wherein said controller determines that a PME# signal is driven in a non-standard manner if the PME# signal is determined to be low at a predetermined time delay after a Power Good signal goes low.

20. The computer system of claim 16, wherein the controller is a power management controller.